

Atty. Docket No. OPP-GZ-2005-0062-US-D0
Serial No: 10/817,096

Amendments to the Figures

Figures 1A-1B have been amended by adding the label "(RELATED ART)" to each Figure, as required by the Examiner. A Replacement Sheet (as required by 37 C.F.R. 1.121(d)) is attached to this Amendment.

Atty. Docket No. OPP-GZ-2005-0062-US-D0
Serial No: 10/817,096

Remarks

Applicant and his representatives wish to thank Examiner Pham for allowing claims 6-12 and 24-40 over the prior art and for the indication that Claim 23 (if rewritten to include all of the limitations of Claim 13) is allowable.

The present invention relates to a method for fabricating a semiconductor device (and in particular, a capacitor). The method (as set forth in Claim 13) generally comprises:

- a) forming an interlayer insulating film having a first trench (a first electrode opening) on a substrate;
- b) forming a first electrode of a capacitor within the first trench;
- c) forming a second trench (a second electrode opening) in the interlayer insulating film adjacent to the first electrode to expose a side of the first electrode;
- d) forming a dielectric layer along inner walls of the second trench; and
- e) forming a second electrode of the capacitor on the dielectric layer to fill the second trench.

The references cited against the originally-filed claims (Stetter et al., U.S. Pat. Appl. Publ. No. 2002/0155676 [hereinafter "Stetter et al."], Toyoda, U.S. Pat. Appl. Publ. No. 2003/0002238 [hereinafter "Toyoda"], and Ohtani et al., U.S. Pat. No. 6,088,070 [hereinafter "Ohtani et al."]) neither disclose nor suggest forming a second trench adjacent to the first electrode *in the insulating film in which the trench for the first electrode was formed* (see step c above). Consequently, the present claims 13-22 are patentable over the cited references.

The Rejection of Claims 13-22 under 35 U.S.C. § 103

The rejection of Claims 13-22 under 35 U.S.C. § 103 as being unpatentable over Stetter et al. in view of Toyoda and Ohtani et al. is respectfully traversed.

Atty. Docket No. OPP-GZ-2005-0062-US-D0
Serial No: 10/817,096

Stetter et al. discloses a MIM capacitor (52) comprising a bottom plate (26), a capacitor dielectric (30) and a top plate (46) (Abstract, ll. 1-2, and FIG. 9). The capacitor bottom plate (26) is formed within an insulating layer (20) for a contact via (32) layer (Abstract, ll. 2-4, and FIG. 9). The capacitor top plate (46) is formed within an insulating layer (34) of a metallization layer (Abstract, ll. 4-6, and FIG. 9). Thus, as a result of forming the bottom and top capacitor plates in different insulating layers (i.e., a contact via insulating layer (20) and a metallization insulating layer (34), respectively), Stetter et al. cannot disclose or suggest forming a second trench adjacent to the first electrode *in the insulating film in which the first trench was formed*. Therefore, Stetter et al. is saliently deficient with regard to the present Claim 13.

Toyoda and Ohtani et al. fail to cure the deficiencies of Stetter et al. with regard to Claim 13.

Toyoda discloses a capacitive moisture sensor including a semiconductor substrate, which has a hole (Abstract, ll. 1-2). A silicon oxide film is located to close the hole, and pair of electrodes is located on the silicon oxide film (Abstract, ll. 2-4). Each electrode is in the shape of a comb, and the electrodes mesh with each other (Abstract, ll. 4-5).

As shown in FIGS. 1-2 of Toyoda, a capacitive moisture sensor S1 includes a semiconductor substrate 10, made of an n-type single crystal silicon and having a front surface and a back surface (also see paragraph [0015]). The substrate 10 has a hole, and a silicon oxide film 20 closes the hole in the substrate 10, as shown in FIG. 2 (see paragraph [0015]). A pair of electrodes 31,32 is located on the silicon oxide film 20 above the hole, and as shown FIG. 1, each electrode 31, 32 is in the shape of a comb (see paragraph [0015]). Toyoda discloses that the electrodes 31, 32 mesh with each other with a predetermined distance to increase the facing area between the electrodes 31, 32 (see paragraph [0015]).

However, Toyoda is silent with regard to forming an electrode in a trench (see Claim 13, which forms two capacitor electrodes in first and second trenches). Consequently, Toyoda cannot possibly suggest forming a second trench adjacent to the first electrode in the insulating film in which the first trench (for the first electrode) was formed.

Atty. Docket No. OPP-GZ-2005-0062-US-D0
Serial No: 10/817,096

Ohtani et al. discloses an active matrix liquid crystal with a capacitor (Title). An auxiliary capacitor is formed by (1) a metal interconnection in the same layer as a source line and (2) a conductive coating serving as a light shield (Abstract, ll. 1-10). Source line 18 and metal interconnection 19 are formed by a known metal wiring forming technique (see col. 4, ll. 49-51 and FIG. 3B). A silicon nitride film 20 is then formed thereon (see col. 4, ll. 54-57 and FIG. 3C). Subsequently, a polyimide layer 21 having a planarized surface is formed by spin coating. In this manner, an interlayer insulating film is formed that consists of the silicon nitride layer 20 and the polyimide layer 21. The polyimide layer 21 is then etched to form an opening 22 for an auxiliary capacitor (see col. 4, ll. 61-67 and FIG. 3C).

Thus, while Ohtani et al. arguably disclose forming a single trench in an insulator film in which a second capacitor electrode is formed, Ohtani et al. is silent with regard to forming two trenches (one adjacent to a capacitor electrode formed in the other) in an insulating film (see Claim 13). Thus, Ohtani et al. cannot disclose or suggest forming a second trench adjacent to the first electrode in the insulating film in which the first trench (for the first electrode) was formed, as is recited in Claim 13.

Thus, Toyoda and Ohtani et al. fail to cure the salient deficiencies of Stetter et al. with regard to the present Claim 13. As a result, no possible combination of the cited references can disclose or suggest forming a second trench adjacent to the first electrode in the insulating film in which the first trench (for the first electrode) was formed, as is recited in Claim 13. Thus, Claim 13 is patentable over the cited references.

Consequently, this ground of rejection is unsustainable, and should be withdrawn.

The Objection to the Drawings

The objection to the drawings has been overcome by appropriate amendment.

Atty. Docket No. OPP-GZ-2005-0062-US-D0
Serial No: 10/817,096

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



Andrew D. Fortney, Ph.D.
Reg. No. 34,600

7257 N. Maple Avenue, Bldg. D, #107
Fresno, California 93720
(559) 299 - 0128